AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

1. (Currently Amended) A magnetic recording/reproduction apparatus, including a recording medium to which an information is recorded to a data sector by a predetermined format, and a magnetic head for recording/reproducing the information, comprising:

a recording/reproducing signal processing circuit for processing the information to be recorded or reproduced;

said format on the medium comprising:

a preamble including additional information for the control of recorded position information, amplitude gain control and data timing recovery;

an information code and a first redundant code ~~composed of plural code sequence blocks~~ used for hard-decision type data error correction, which are composed of ~~a plural code block~~plural code sequence blocks;

a second redundant code used for soft-decision type error correction for each code sequence block, which is inserted in predetermined positions in each code sequence block.

2. (Previously Presented) The magnetic recording/reproducing apparatus according to claim 1, wherein:

said first redundant code is a Reed-Solomon code, and

said second redundant code is a Turbo code.

3. (Currently Amended) A recording/reproducing signal processing circuit including a recording signal processing system and a reproducing signal processing system, which is utilized for a storage recording/reproducing that reproduces an information code sequence consisting of a plurality of code bits recorded by a predetermined unit in a recording medium, said recording signal processing system comprising:

a first encoding circuit that applies first error-correction coding to the information code sequence by the predetermined unit, and adds a first redundant code sequence to said coded information code sequence, thereby generates an error-correction code sequence;

a concatenated encoder that:

divides the error-correction code sequence output from the first encoding circuit into continuous plural code sequence blocks having predetermined length,

stores ~~the plural code sequence blocks~~each code sequence block,

executes second error-correction coding for each code sequence block, and

generates a second redundant code sequence with referring to the contents of each code sequence block; and

a code switch that outputs the plural code sequence blocks and the second redundant code sequence alternatively, thereby generating the information code sequence comprised of the plural code sequence blocks;

wherein the second redundant code is inserted in ~~the~~ each code sequence block.

4. (Currently Amended) The recording/reproducing signal processing circuit according to claim 3, wherein said concatenated encoder comprises:

a code permutation circuit that permutes code bits in ~~the divided~~ each code sequence block, and stores the ~~plural~~ permuted code sequence blocks;

a second encoding circuit that executes second error-correction coding for each code sequence block, and generates a second redundant code sequence, referring to the contents of each code sequence block stored in the code permutation circuit.

5. (Currently Amended) The recording/reproducing signal processing circuit according to claim 4, said recording/reproducing signal processing system comprising:

a maximum-likelihood detector that receives a reproduced signal sequence supplied from the recording medium and outputs the soft-output code information sequence, which is comprised of multi-valued reliability information corresponding to ~~a reliability code bit~~each code bit of the information code sequence;

a multiplexer that divides the soft-output code information sequence into a first soft-output code information corresponding to the information code sequence ~~other than the first redundant code and the second redundant code~~ of the plural code

sequence blocks and a second soft-output code information corresponding to the second redundant code inserted in each code sequence block;

a plurality of soft-output buffers that store the first soft-output code information and the second redundant code;

an iterative detector that executes an error-correction to the first soft-output code information in each code sequence block by using the second soft-output code information, and outputs an error-correction decoded sequence; and

an error-correction demodulator that corrects a code error in the error-correction decoded sequence by using the first redundant code.

6. (Currently Amended) The recording/reproducing signal processing circuit according to claim 5, said iterative detector further comprising a parity decoder that executes said error-correction in each code sequence block by updating ~~the code bit of~~ the first soft-output code information ~~to more reliable code bit~~ using the second soft-output code information.

7. (Previously Presented) The recording/reproducing signal processing circuit according to claim 5, wherein the error-correction by the iterative detector or the error-correction demodulator is repeated only in case code errors are detected and all the detected code errors cannot be corrected.

8. – 13. (Cancelled)

14. (Previously Presented) An integrated circuit comprising a recording/reproducing signal processing circuit according to claim 3.

15. (Previously Presented) A magnetic hard disk drive apparatus comprising a recording/reproducing signal processing circuit according to claim 3.

16. (Currently Amended) The magnetic recording/reproduction apparatus according to claim 1, wherein:

the number of code symbols of the code sequence block is equal or less than a maximum number of error code symbols that can be corrected by the first redundant code.

17. (Currently Amended) The recording/reproducing signal processing circuit according to claim 3, wherein:

the code symbol length of the code sequence block is equal or less than a maximum number of error code symbols that can be corrected by the first redundant code.

18. (New) The recording/reproducing signal processing circuit according to claim 5, wherein:

the iterative decoder iteratively feedbacks the first soft-output code information corrected by itself into the maximum-likelihood decoder.

19. (New) The recording/reproducing signal processing circuit according to claim 5, wherein:

the maximum-likelihood decoder outputs the soft-output code information through a permutation circuit, and

the iterative decoder feedbacks the first soft-output code information corrected by itself into the maximum-likelihood decoder through the inverted permutation circuit.

20. (New) The recording/reproducing signal processing circuit according to claim 5, wherein:

said iterative decoder comprises multiple parity decoders, and each of the said parity decoders inputs the first soft-output code information updated by the other parity decoder through the permutation circuit or the inverted permutation circuit, and alternately and iteratively executes said error-correction in each code sequence block by updating the input first soft-output code sequence block by updating the input first soft-output code information using the second soft-output code information.